In the Specification

Please amend the specification of this application as follows:

Rewrite the paragraph at page 1 lines 15 to 16 as follows:

--U.S. Provisional Application No. ~~60/___,___ (TI-29494)~~ 60/224,607 filed August 11, 2000 entitled DATAPIPE ROUTING BRIDGE, now U.S. Patent Application No. 09/905,378 filed July 13, 2001; and--

Rewrite the paragraph at page 1, lines 17 to 19 as follows:

--U.S. Provisional Application No. ~~60/___,___ (TI-29499)~~ 60/224,586 filed August 11, 2002 entitled MULTIPROCESSOR NETWORK NODE FAILURE DETECTION AND RECOVERY, now U.S. Patent Application No. 09/904,991 filed July 13, 2001.--

Rewrite the paragraph at page 10, lines 11 to 25 as follows:

--Figure 4 illustrates the datapipe within a conventional digital signal processor integrated circuit. Internal I/O RAM input buffers 405, when almost full, send an event to the chip direct memory access (DMA) unit to move the data into the level-2 (L2) main memory 401, where it can be accessed directly by the central processing unit core 400. Note that this application contemplates that central processing unit core 400 is a digital signal processor, however this invention is equally applicable to a general purpose data processor. Internal I/O RAM 405 of the datapipe is split into two independent blocks for simultaneous direct memory access unit and datapipe access. The direct memory access port servicing internal I/O RAM ~~406~~ 405 and the datapipe looks exactly like the other direct memory access ports driving the remaining chip peripherals.--